Sierra Components, Inc.

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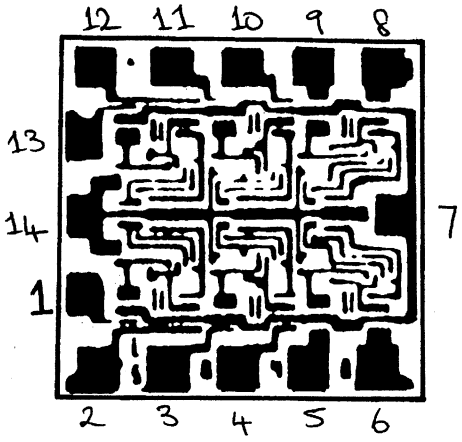
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



Pad	Function	Pad	Function
1	1A	8	4Y
2	1Y	9	4A
3	2A	10	5Y
4	2Y	11	5A
5	3A	12	6Y
6	3Y	13	6A
7	GND	14	V_{CC}

Topside Metal: Al
Backside: Si
Backside Potential: Gnd
Mask Ref: C
Bond Pads (Mils): 4 x 4

APPROVED BY:
MFG: Texas Inst

DIE SIZE (Mils): 40 x 37
THICKNESS: 15

DATE: 3/10/99
P/N: SN74LS04

DG 10.1.2
Rev A 3-4-99